ETCHANT FOR SIGNAL WIRE AND METHOD OF MANUFACTURING THIN FILM TRANSISTOR ARRAY PANEL USING ETCHANT

BACKGROUND OF THE INVENTION

(a) Field of the Invention

[0001] The present invention relates to an etchant for a signal wire and a manufacturing method of a thin film transistor array panel using an etchant.

(b) Description of the Related Art

[0002] Liquid crystal displays (LCDs) are one of the most widely used flat panel displays. An LCD includes two panels provided with field-generating electrodes and a liquid crystal (LC) layer interposed therebetween. The LCD displays images by applying voltages to the field-generating electrodes to generate an electric field in the LC layer, which determines orientations of LC molecules in the LC layer to adjust polarization of incident light.

[0003] Among LCDs including field-generating electrodes on respective panels, a kind of LCDs provides a plurality of pixel electrodes arranged in a matrix at one panel and a common electrode covering an entire surface of the other panel. The image display of the LCD is accomplished by applying individual voltages to the respective pixel electrodes. For the application of the individual voltages, a plurality of three-terminal thin film transistors (TFTs) are connected to the respective pixel electrodes, and a plurality of gate lines transmitting signals for controlling the TFTs and a plurality of data lines transmitting voltages to be applied to the pixel electrodes are provided on the panel.

[0004] The panel for an LCD has a layered structure including several conductive layers and several insulating layers. The gate lines, the data lines, and the pixel electrodes are made from different conductive layers (referred to as "gate conductor," "data conductor," and "pixel conductor" hereinafter) preferably deposited in sequence and separated by insulating layers. A

TFT includes three electrodes: a gate electrode made from the gate conductor and source and drain electrodes made from the data conductor. The source electrode and the drain electrode are connected by a semiconductor usually located thereunder, and the drain electrode is connected to the pixel electrode through a hole in an insulating layer.

[0005] The gate conductor and the data conductor are preferably made of Al containing metal such as Al and Al alloy having low resistivity for reducing the signal delay in the gate lines and the data lines. The data conductor also includes a refractory metal for good contact with the semiconductor. The pixel electrodes are usually made of transparent conductive material such as indium tin oxide (ITO) for both the field generation upon voltage application and the light transmission.

[0006] In the meantime, the conductors are patterned by dry etching or wet etching with an etchant. An etchant for patterning dual layers of Al (or Al-Nd alloy) and Mo is disclosed in Korean Patent Application Publication No. 2001-75932, an etchant for patterning triple layers of Mo, Al (or Al-Nd alloy), and Mo is disclosed in Korean Patent Application Publication Serial No. 2001-91799, and an etchant for patterning a layer of ITO is disclosed in Korean Patent Application Publication Serial No. 2002-33025.

[0007] Since different layers are etched using different etching conditions, the manufacturing process is complicated and the manufacturing cost is expensive.

SUMMARY OF THE INVENTION

[0008] A method of manufacturing a thin film transistor array panel is provided, the method includes: forming a gate conductor on an insulating substrate; forming a gate insulating layer; forming a semiconductor member; forming a data conductor; and forming a pixel electrode connected to the drain electrode, wherein the gate conductor, the data conductor, and the pixel electrode are formed using a single etchant.

[0009] The etchant preferably contains about 50-60% H_3PO_4, about 6-10% HNO_3, about 15-25% CH_3COOH, about 2-5% stabilizer, and deionized water. The stabilizer may contain oxy-hydride inorganic acid represented by $M(OH)_XL_Y$, where M includes at least one of Zn, Sn, Cr, Al, Ba, Fe, Ti, Si and B, L includes at least one of H_2O, NH_3, CN and NH_2R (where R is alkyl group), X is 2 or 3, and Y is 0, 1, 2 or 3.

[0010] The gate conductor preferably includes a lower film of Al or Al alloy, more preferably Al-Nd, and an upper film of Mo or Mo alloy, more preferably MoW.

[0011] The data conductor preferably includes Mo or Mo alloy, and the pixel electrode preferably includes IZO.

[0012] The lower layer of the gate conductor, the upper layer of the gate conductor, the data conductor, and the pixel electrode may have thickness of about 1,500-3,000 Å, about 300-600 Å, about 1,500-3,000 Å, and about 800-1,000 Å, respectively.

[0013] The etchant preferably contains about 65-75% H_3PO_4, about 0.5-4% HNO_3, about 9-13% CH_3COOH, about 2-5% stabilizer, and deionized water. The stabilizer may contain oxy-hydride inorganic acid represented by $M(OH)_XL_Y$, where M includes at least one of Zn, Sn, Cr, Al, Ba, Fe, Ti, Si and B, L includes at least one of H_2O, NH_3, CN and NH_2R (where R is alkyl group), X is 2 or 3, and Y is 0, 1, 2 or 3.

[0014] The gate conductor preferably includes a lower film of Al or Al alloy, more preferably Al-Nd, and an upper film of Mo.

[0015] The data conductor preferably includes a bottom layer of Mo, an intermediate layer of Al or Al alloy, and a top layer of Mo, and the pixel electrode preferably includes IZO.

[0016] A method of manufacturing a thin film transistor array panel is provided, which includes: forming a gate conductor on an insulating substrate; forming a gate insulating layer;

forming a semiconductor member; forming a data conductor; and forming a pixel electrode connected to the drain electrode, wherein at least one of the gate conductor, the data conductor, and the pixel electrode are formed by using an etchant including a phosphoric acid of about 50-60%, a nitric acid of about 6-10%, an acetic acid of about 15-25%, a stabilizer of about 2-5% stabilizer, and deionized water, or an etchant including a phosphoric acid of about 65-75%, a nitric acid of about 0.5-4%, an acetic acid of about 9-13%, a stabilizer of about 2-5% stabilizer, and deionized water, where the stabilizer includes oxy-hydride inorganic acid represented by $M(OH)_XL_Y$, where M includes at least one of Zn, Sn, Cr, Al, Ba, Fe, Ti, Si and B, L includes at least one of H_2O, NH_3, CN and NH_2R (where R is alkyl group), X is 2 or 3, and Y is 0, 1, 2 or 3.

[0017] At least two of the gate conductor, the data conductor, and the pixel electrode preferably include at least one of Mo, Mo alloy, Al, Al alloy, and IZO, and furthermore, each of the gate conductor, the data conductor, and the pixel electrode may include at least one of Mo, Mo alloy, Al, Al alloy, and IZO.

[0018] An etchant for a signal wire according to an embodiment of the present invention includes: a phosphoric acid of about 50-60%; a nitric acid of about 6-10%; an acetic acid of about 15-25%; a stabilizer of about 2-5% stabilizer; and deionized water, wherein the stabilizer includes oxy-hydride inorganic acid represented by $M(OH)_XL_Y$, where M includes at least one of Zn, Sn, Cr, Al, Ba, Fe, Ti, Si and B, L includes at least one of H_2O, NH_3, CN and NH_2R (where R is alkyl group), X is 2 or 3, and Y is 0, 1, 2 or 3.

[0019] An etchant for a signal wire according to another embodiment of the present invention includes: a phosphoric acid of about 65-75%; a nitric acid of about 0.5-4%; an acetic acid of about 9-13%; a stabilizer of about 2-5% stabilizer; and deionized water, wherein the stabilizer includes oxy-hydride inorganic acid represented by $M(OH)_XL_Y$, where M includes at

least one of Zn, Sn, Cr, Al, Ba, Fe, Ti, Si and B, L includes at least one of H_2O, NH_3, CN and NH_2R (where R is alkyl group), X is 2 or 3, and Y is 0, 1, 2 or 3.

[0020] The etchant may be used for patterning an Al or Al alloy layer, a Mo or Mo alloy layer, and multiple layers including an Al or Al alloy layer and a Mo or Mo alloy layer, and it may also be used for patterning an IZO layer.

[0021] The etchant may be used for patterning multiple layers including a Mo layer, an Al or Al alloy layer, and a Mo layer deposited in sequence.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The present invention will become more apparent by describing embodiments thereof in detail with reference to the accompanying drawings in which:

[0023] Figs. 1-3 are photographs of sections of signal wires etched by a single etchant according to an embodiment of the present invention;

[0024] Fig. 4 is a layout view of an exemplary TFT array panel for an LCD according to an embodiment of the present invention;

[0025] Fig. 5 is a sectional view of the TFT array panel shown in Fig. 4 taken along the line V-V';

[0026] Figs. 6A, 7A, 8A and 9A are layout views of the TFT array panel shown in Figs. 4 and 5 in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention;

[0027] Figs. 6B, 7B, 8B and 9B are sectional views of the TFT array panel shown in Figs. 6A, 7A, 8A and 9A taken along the lines VIB-VIB', VIIB-VIIB', VIIIB-VIIIB', and IXB-IXB', respectively;

[0028] Fig. 10 is a layout view of an exemplary TFT array panel for an LCD according to another embodiment of the present invention;

[0029] Figs. 11 and 12 are sectional views of the TFT array panel shown in Fig. 10 taken along the line XI-XI' and the line XII-XII', respectively;

[0030] Fig. 13A is a layout view of a TFT array panel shown in Figs. 10-12 in the first step of a manufacturing method thereof according to an embodiment of the present invention;

[0031] Figs. 13B and 13C are sectional views of the TFT array panel shown in Fig. 13A taken along the lines XIIIB-XIIIB' and XIIIC-XIIIC', respectively;

[0032] Figs. 14A and 14B are sectional views of the TFT array panel shown in Fig. 13A taken along the lines XIIIB-XIIIB' and XIIIC-XIIIC', respectively, and illustrate the step following the step shown in Figs. 13B and 13C;

[0033] Fig. 15A is a layout view of the TFT array panel in the step following the step shown in Figs. 14A and 14B;

[0034] Figs. 15B and 15C are sectional views of the TFT array panel shown in Fig. 15A taken along the lines XVB-XVB' and XVC-XVC', respectively;

[0035] Figs. 16A, 17A and 18A and Figs. 16B, 17B and 18B are respective sectional views of the TFT array panel shown in Fig. 15A taken along the lines XVB-XVB' and XVC-XVC', respectively, and illustrate the steps following the step shown in Figs. 15B and 15C;

[0036] Fig. 19A is a layout view of a TFT array panel in the step following the step shown in Figs. 18A and 18B;

[0037] Figs. 19B and 19C are sectional views of the TFT array panel shown in Fig. 19A taken along the lines XIXB-XIXB' and XIXC-XIXC', respectively;

[0038] Fig. 20 is a layout view of an exemplary TFT array panel for an LCD according to another embodiment of the present invention;

[0039] Fig. 21 is a sectional view of the TFT array panel shown in Fig. 20 taken along

the line XXI-XXI';

[0040] Figs. 22A, 23A, 24A and 25A are layout views of the TFT array panel shown in Figs. 20 and 21 in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention; and

[0041] Figs. 22B, 23B, 24B and 25B are sectional views of the TFT array panel shown in Figs. 22A, 23A, 24A and 25A taken along the lines XXIIB-XXIIB', XXIIIB-XXIIIB', XXIVB-XXIVB', and XXV-XXV', respectively.

DETAILED DESCRIPTION OF EMBODIMENTS

[0042] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

[0043] In the drawings, the thickness of layers, films and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0044] Now, etchants for a wire, TFT array panels and manufacturing methods thereof according to embodiments of the present invention will be described with reference to the accompanying drawings.

[0045] Figs. 1-3 are photographs of sections of signal wires etched by a single etchant according to an embodiment of the present invention.

[0046] A conductive layer was deposited on a substrate and etched using an etchant

contains about 55% phosphoric acid (H_3PO_4), about 8% nitric acid (HNO_3), about 19% acetic acid (CH_3COOH), about 3% stabilizer, and deionized water. The stabilizer includes oxy-hydride inorganic acid represented by $M(OH)_XL_Y$, where M is Zn, Sn, Cr, Al, Ba, Fe, Ti, Si or B, L is H_2O, NH_3, CN or NH_2R (where R is alkyl group), X is 2 or 3, and Y is 0, 1, 2 or 3.

[0047] Referring to Fig. 1, the conductive layer includes a lower Al-Nd alloy layer having a thickness of about 2,500 Å and an upper MoW alloy layer of about 500 Å and the substrate was dipped into the etchant for etching the conductive layer. The photograph shows that the etched lateral side of the conductive layer has an inclination angle (or taper angle) of 40-50 degrees with respect to the surface of the substrate.

[0048] Referring to Fig. 2, the conductive layer is made of MoW alloy and has a thickness of about 2,000 Å and the etchant was sprayed over the substrate for etching the conductive layer. The photograph shows that the etched lateral side of the conductive layer has an inclination angle of 30-40 degrees with respect to the surface of the substrate.

[0049] Referring to Fig. 3, the conductive layer is made of IZO and has a thickness of about 900 Å and the etchant was sprayed over the substrate for etching the conductive layer. The photograph shows that the etched lateral side of the conductive layer has an inclination angle of 25-30 degrees with respect to the surface of the substrate.

[0050] Consequently, the conductive layers made of Al-Nd alloy, MoW alloy, and IZO are etched by a single etchant such that the inclination angles of the later sides of the conductive layers ranges from about 25 degrees to about 50 degrees.

[0051] A TFT array panel for an LCD will be described in detail with reference to Figs. 4 and 5.

[0052] Fig. 4 is an exemplary layout view of TFTs, pixel electrodes, portions of signal

lines located on the display area and expansions of the signal lines located on the peripheral area of the exemplary TFT array panel shown in Fig. 2 according to an embodiment of the present invention, and Fig. 5 is a sectional view of the TFT array panel shown in Fig. 4 taken along the line V-V'.

[0053] A plurality of gate lines 121 for transmitting gate signals are formed on an insulating substrate 110. Each gate line 121 extends substantially in a transverse direction and a plurality of portions of each gate line 121 form a plurality of gate electrodes 123. Each gate line 121 includes a plurality of projections 127 protruding downward and an expansion 125 having wider width for contact with another layer or an external device.

[0054] The gate lines 121 include two films having different physical characteristics, a lower film 121p and an upper film 121q. The lower film 121p is preferably made of low resistivity metal including Al containing metal such as Al and Al alloy for reducing signal delay or voltage drop in the gate lines 121. On the other hand, the upper film 121q is preferably made of material such as Mo and Mo alloy, which has good physical, chemical, and electrical contact characteristics with other materials such as indium tin oxide (ITO) and indium zinc oxide (IZO). A good exemplary combination of the lower film material and the upper film material is Al-Nd alloy and Mo-W alloy. In Fig. 5, the lower and the upper films of the gate electrodes 123 are indicated by reference numerals 123p and 123q, respectively, the lower and the upper films of the projections 127 are indicated by reference numerals 127p and 127q, and the lower and the upper films of the expansions 125 are indicated by reference numerals 125p and 125q, respectively. However, the expansions 125 of the gate lines 121 include only a lower film.

[0055] In addition, the lateral sides of the upper film 121q and the lower film 121p are tapered, and the inclination angle of the lateral sides with respect to a surface of the substrate 110

ranges about 20-80 degrees.

[0056] A gate insulating layer 140 preferably made of silicon nitride (SiNx) is formed on the gate lines 121.

[0057] A plurality of semiconductor stripes 151 preferably made of hydrogenated amorphous silicon (abbreviated to "a-Si") are formed on the gate insulating layer 140. Each semiconductor stripe 151 extends substantially in the longitudinal direction and has a plurality of projections 154 branched out toward the gate electrodes 123. The width of each semiconductor stripe 151 becomes large near the gate lines 121 such that the semiconductor stripe 151 covers large areas of the gate lines 121.

[0058] A plurality of ohmic contact stripes and islands 161 and 165 preferably made of silicide or n+ hydrogenated a-Si heavily doped with n type impurity are formed on the semiconductor stripes 151. Each ohmic contact stripe 161 has a plurality of projections 163, and the projections 163 and the ohmic contact islands 165 are located in pairs on the projections 154 of the semiconductor stripes 151.

[0059] The lateral sides of the semiconductor stripes 151 and the ohmic contacts 161 and 165 are tapered, and the inclination angles thereof are preferably in a range between about 30-80 degrees.

[0060] A plurality of data lines 171, a plurality of drain electrodes 175, and a plurality of storage capacitor conductors 177 are formed on the ohmic contacts 161 and 165 and the gate insulating layer 140.

[0061] The data lines 171 for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines 121. Each data line 171 includes an expansion 179 having wider width for contact with another layer or an external device.

[0062] A plurality of branches of each data line 171, which project toward the drain electrodes 175, form a plurality of source electrodes 173. Each pair of the source electrodes 173 and the drain electrodes 175 are separated from each other and opposite each other with respect to a gate electrode 123. A gate electrode 123, a source electrode 173, and a drain electrode 175 along with a projection 154 of a semiconductor stripe 151 form a TFT having a channel formed in the projection 154 disposed between the source electrode 173 and the drain electrode 175.

[0063] The storage capacitor conductors 177 overlap the projections 127 of the gate lines 121.

[0064] The data lines 171, the drain electrodes 175, and the storage capacitor conductors 177 is preferably made of Mo or Mo alloy, and more preferably, it is made of Mo-W alloy. They may include an upper film (not shown) preferably made of Mo, Mo alloy and an underlying lower film (not shown) preferably made of Al containing metal. In addition, they may further include a Mo or Mo alloy film disposed under the Al containing metal film.

[0065] Like the gate lines 121, the data lines 171, the drain electrodes 175, and the storage capacitor conductors 177 have tapered lateral sides, and the inclination angles thereof range about 30-80 degrees.

[0066] The ohmic contacts 161 and 165 are interposed only between the underlying semiconductor stripes 151 and the overlying data lines 171 and the overlying drain electrodes 175 thereon and reduce the contact resistance therebetween. The semiconductor stripes 151 include a plurality of exposed portions, which are not covered with the data lines 171 and the drain electrodes 175, such as portions located between the source electrodes 173 and the drain electrodes 175. Although the semiconductor stripes 151 are narrower than the data lines 171 at most places, the width of the semiconductor stripes 151 becomes large near the gate lines 121 as

described above, to smooth the profile of the surface, thereby preventing the disconnection of the data lines 171.

[0067] A passivation layer 180 is formed on the data lines 171, the drain electrodes 175, the storage conductors 177, and the exposed portions of the semiconductor stripes 151. The passivation layer 180 is preferably made of photosensitive organic material having a good flatness characteristic, low dielectric insulating material having dielectric constant lower than 4.0 such as a-Si:C:O and a-Si:O:F formed by plasma enhanced chemical vapor deposition (PECVD), or inorganic material such as silicon nitride. The passivation layer 180 may have a dual layered structure including an inorganic lower layer preferably made of silicon nitride and an organic upper layer such that the exposed portions of the semiconductor stripes 151 is in contact with the inorganic layer. Furthermore, the thick organic insulating layer is removed in a peripheral area provided with the expansions 125 and 179 of the gate lines 121 and the data lines 179 for smooth contact between the expansions 125 and 179 and external driving circuits and this configuration is particularly advantageous for a COG (chip on glass) type mounting.

[0068] The passivation layer 180 has a plurality of contact holes 185, 187 and 189 exposing the lower films 175p of the drain electrodes 175, the lower films 177p of the storage conductors 177, and the expansions 179 of the data lines 171, respectively. The passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 182 exposing the expansions 125 of the gate lines 121. Figs. 4 and 5 shows that the contact holes 182, 185, 187 and 189 have inclined sidewalls.

[0069] A plurality of pixel electrodes 190 and a plurality of contact assistants 92 and 97, which are preferably made of IZO, are formed on the passivation layer 180.

[0070] The pixel electrodes 190 are physically and electrically connected to the drain

electrodes 175 through the contact holes 185 and to the storage capacitor conductors 177 through the contact holes 187 such that the pixel electrodes 190 receive the data voltages from the drain electrodes 175 and transmit the received data voltages to the storage capacitor conductors 177.

[0071] The pixel electrodes 190 supplied with the data voltages generate electric fields in cooperation with a common electrode (not shown) on another panel (not shown), which reorient liquid crystal molecules in a liquid crystal layer (not shown) disposed therebetween.

[0072] A pixel electrode 190 and a common electrode form a liquid crystal capacitor, which stores applied voltages after turn-off of the TFT. An additional capacitor called a "storage capacitor," which is connected in parallel to the liquid crystal capacitor, is provided for enhancing the voltage storing capacity. The storage capacitors are implemented by overlapping the pixel electrodes 190 with the gate lines 121 adjacent thereto (called "previous gate lines"). The capacitances of the storage capacitors, i.e., the storage capacitances are increased by providing the projections 127 at the gate lines 121 for increasing overlapping areas and by providing the storage capacitor conductors 177, which are connected to the pixel electrodes 190 and overlap the projections 127, under the pixel electrodes 190 for decreasing the distance between the terminals.

[0073] The pixel electrodes 190 overlap the gate lines 121 and the data lines 171 to increase aperture ratio but it is optional.

[0074] The contact assistants 92 and 97 are connected to the exposed expansions 125 of the gate lines 121 and the exposed expansions 179 of the data lines 171 through the contact holes 182 and 189, respectively. The contact assistants 92 and 97 are not requisites but preferred to protect the exposed portions 125 and 179 and to complement the adhesiveness of the exposed portions 125 and 179 and external devices.

[0075] According to another embodiment of the present invention, a plurality of metal islands (not shown) are formed near the expansions 125 and 129 of the gate lines 121 and the data lines 179 and they are connected to the contact assistants 92 and 97 through a plurality of contact holes (not shown) are formed in the passivation layer 180 and/or the gate insulating layer 140.

[0076] A method of manufacturing the TFT array panel shown in Figs. 4 and 5 according to an embodiment of the present invention will be now described in detail with reference to Figs. 6A to 9B as well as Figs. 4 and 5.

[0077] Figs. 6A, 7A, 8A and 9A are layout views of the TFT array panel shown in Figs. 4 and 5 in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention, and Figs. 6B, 7B, 8B and 9B are sectional views of the TFT array panel shown in Figs. 6A, 7A, 8A and 9A taken along the lines VIB-VIB', VIIB-VIIB', VIIIB-VIIIB', and IXB-IXB', respectively.

[0078] Two conductive films, a lower conductive film and an upper conductive film are sputtered in sequence on an insulating substrate 110 such as transparent glass. The lower conductive film has a thickness of about 1,500-3,000 Å, preferably 2,500 Å, and is made of Al-Nd alloy, while the upper conductive film has a thickness of about 300-600 Å, preferably 500 Å, and is made of Mo-W alloy.

[0079] Referring to Figs. 6A and 6B, the upper conductive film and the lower conductive film are simultaneously patterned by photolithography and wet etch with an etchant to form a plurality of gate lines 121 including a plurality of gate electrodes 123, a plurality of projections 127, and a plurality of expansions 125. The etchant contains about 50-60% phosphoric acid (H_3PO_4), about 6-10% nitric acid (HNO_3), about 15-25% acetic acid (CH_3COOH), about 2-5%

stabilizer, and deionized water. The stabilizer includes oxy-hydride inorganic acid represented by $M(OH)_XL_Y$, where M is Zn, Sn, Cr, Al, Ba, Fe, Ti, Si or B, L is H_2O, NH_3, CN or NH_2R (where R is alkyl group), X is 2 or 3, and Y is 0, 1, 2 or 3.

[0080] Referring to Figs. 7A and 7B, after sequential deposition of a gate insulating layer 140, an intrinsic a-Si layer, and an extrinsic a-Si layer, the extrinsic a-Si layer and the intrinsic a-Si layer are photo-etched to form a plurality of extrinsic semiconductor stripes 164 and a plurality of intrinsic semiconductor stripes 151 including a plurality of projections 154 on the gate insulating layer 140.

[0081] Referring to Figs. 8A and 8B, a conductive film made of Mo-W alloy and having a thickness of about 1,500-3,000 Å, preferably 2,000 Å, is deposited and wet-etched with the etchant used for patterning the gate lines 121 to form a plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of expansions 179, a plurality of drain electrodes 175, and a plurality of storage capacitor conductors 177.

[0082] Thereafter, portions of the extrinsic semiconductor stripes 164, which are not covered with the data lines 171, the drain electrodes 175, and the storage capacitor conductors 177, are removed to complete a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 and to expose portions of the intrinsic semiconductor stripes 151. Oxygen plasma treatment preferably follows thereafter in order to stabilize the exposed surfaces of the semiconductor stripes 151.

[0083] Next, a passivation layer 180 is formed by depositing silicon nitride, by PECVD of low dielectric material such as a-Si:C:O or a-Si:O:F, or by coating a photosensitive organic insulating material having a good planarization characteristic. Referring to Figs. 9A and 9B, the passivation layer 180 as well as the gate insulating layer 140 is photo-etched to form a plurality

of contact holes 182, 185, 187 and 189 exposing the expansions 125 of the gate lines 121, the drain electrodes 175, the storage capacitor conductors 177, and the expansions 179 of the data lines 171.

[0084] Finally, as shown in Figs. 4 and 5, a plurality of pixel electrodes 190 and a plurality of contact assistants 92 and 97 are formed on the passivation layer 180 by sputtering and photo-etching an IZO layer having a thickness of about 800-1,000 Å, preferably about 900 Å with the etchant used for etching the gate lines 121 and the data lines 175.

[0085] In the manufacturing method of the TFT array panel according to this embodiment, the gate lines 121, the data lines 171, and the pixel electrodes 190 are etched by using a single etchant. Accordingly, the manufacturing method and apparatus are simplified, thereby reducing the manufacturing cost.

[0086] A TFT array panel for an LCD according to another embodiment of the present invention will be described in detail with reference to Figs. 10-12.

[0087] Fig. 10 is a layout view of an exemplary TFT array panel for an LCD according to another embodiment of the present invention, and Figs. 11 and 12 are sectional views of the TFT array panel shown in Fig. 10 taken along the line XI-XI' and the line XII-XII', respectively.

[0088] As shown in Figs. 10-12, a layered structure of a TFT array panel of an LCD according to this embodiment is almost the same as that shown in Figs. 4 and 5. That is, a plurality of gate lines 121 including a plurality of gate electrodes 123 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain

electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of contact holes 182, 185 and 189 are provided at the passivation layer 180 and/or the gate insulating layer 140, and a plurality of pixel electrodes 190 and a plurality of contact assistants 92 and 97 are formed on the passivation layer 180.

[0089] Different from the TFT array panel shown in Figs. 4 and 5, the TFT array panel according to this embodiment provides a plurality of storage electrode lines 131, which are separated from the gate lines 121 and have a plurality of expansions 133, on the same layer as the gate lines 121 without projections. The storage electrode lines 131 are supplied with a predetermined voltage such as the common voltage. Without providing the storage capacitor conductors 177 shown in Figs. 4 and 5, the drain electrodes 175 extend to overlap the storage electrode lines 131 to form storage capacitors. The storage electrode lines 131 may be omitted if the storage capacitance generated by the overlapping of the gate lines 121 and the pixel electrodes 190 is sufficient. The positions of the storage electrode lines 131 may be changed, and, for example, the storage electrode lines 131 are disposed near the edges of the pixel electrodes 190 in consideration of the aperture ratio.

[0090] Furthermore, the gate lines 125 and the storage electrode lines 131 have a single layered structure.

[0091] The semiconductor stripes 151 have almost the same planar shapes as the data lines 171 and the drain electrodes 175 as well as the underlying ohmic contacts 161 and 165, except for the projections 154 where TFTs are provided. That is, the semiconductor stripes 151 include some exposed portions, which are not covered with the data lines 171 and the drain electrodes 175, such as portions located between the source electrodes 173 and the drain electrodes 175.

[0092] Now, a method of manufacturing the TFT array panel shown in Figs. 10-12 according to an embodiment of the present invention will be described in detail with reference to Figs. 13A-19C as well as Figs. 10-12.

[0093] Fig. 13A is a layout view of a TFT array panel shown in Figs. 10-12 in the first step of a manufacturing method thereof according to an embodiment of the present invention; Figs. 13B and 13C are sectional views of the TFT array panel shown in Fig. 13A taken along the lines XIIIIB-XIIIIB' and XIIIIC-XIIIIC', respectively; Figs. 14A and 14B are sectional views of the TFT array panel shown in Fig. 13A taken along the lines XIIIB-XIIIB' and XIIIC-XIIIC', respectively, and illustrate the step following the step shown in Figs. 13B and 13C; Fig. 15A is a layout view of the TFT array panel in the step following the step shown in Figs. 14A and 14B; Figs. 15B and 15C are sectional views of the TFT array panel shown in Fig. 15A taken along the lines XVB-XVB' and XVC-XVC', respectively; Figs. 16A, 17A and 18A and Figs. 16B, 17B and 18B are respective sectional views of the TFT array panel shown in Fig. 15A taken along the lines XVB-XVB' and XVC-XVC', respectively, and illustrate the steps following the step shown in Figs. 15B and 15C; Fig. 19A is a layout view of a TFT array panel in the step following the step shown in Figs. 18A and 18B; and Figs. 19B and 19C are sectional views of the TFT array panel shown in Fig. 19A taken along the lines XIXB-XIXB' and XIXC-XIXC', respectively..

[0094] Referring to Figs. 13A-13C, a plurality of gate lines 121 including a plurality of gate electrodes 123 and a plurality of storage electrode lines 131 are formed on a substrate 110 by photo etching using an etchant. The etchant about 50-60% H_3PO_4, about 6-10% HNO_3, about 15-25% CH_3COOH, about 2-5% stabilizer, and deionized water. The stabilizer includes oxy-hydride inorganic acid represented by $M(OH)_XL_Y$, where M is Zn, Sn, Cr, Al, Ba, Fe, Ti, Si or B, L is H_2O, NH_3, CN or NH_2R (where R is alkyl group), X is 2 or 3, and Y is 0, 1, 2 or 3.

[0095] As shown in Figs. 14A and 14B, a gate insulating layer 140, an intrinsic a-Si layer 150, and an extrinsic a-Si layer 160 are sequentially deposited by CVD such that the layers 140, 150 and 160 have thickness of about 1,500-5,000 Å, about 500-2,000 Å and about 300-600 Å, respectively. A conductive layer 170 having a thickness of about 1,500-3,000 Å and made of Mo or Mo alloy such as MoW is deposited by sputtering, and a photoresist film 210 with the thickness of about 1-2 microns is coated on the conductive layer 170.

[0096] The photoresist film 210 is exposed to light through an exposure mask (not shown), and developed such that the developed photoresist has a position dependent thickness. The photoresist shown in Figs. 15B and 15C includes a plurality of first to third portions with decreased thickness. The first portions located on wire areas A and the second portions located on channel areas C are indicated by reference numerals 212 and 214, respectively, and no reference numeral is assigned to the third portions located on remaining areas B since they have substantially zero thickness to expose underlying portions of the conductive layer 170. The thickness ratio of the second portions 214 to the first portions 212 is adjusted depending upon the process conditions in the subsequent process steps. It is preferable that the thickness of the second portions 214 is equal to or less than half of the thickness of the first portions 212, and in particular, equal to or less than 4,000 Å.

[0097] The position-dependent thickness of the photoresist is obtained by several techniques, for example, by providing translucent areas on the exposure mask 300 as well as transparent areas and light blocking opaque areas. The translucent areas may have a slit pattern, a lattice pattern, a thin film(s) with intermediate transmittance or intermediate thickness. When using a slit pattern, it is preferable that the width of the slits or the distance between the slits is smaller than the resolution of a light exposer used for the photolithography. Another example is

to use reflowable photoresist. In detail, once a photoresist pattern made of a reflowable material is formed by using a normal exposure mask only with transparent areas and opaque areas, it is subject to reflow process to flow onto areas without the photoresist, thereby forming thin portions.

[0098] The different thickness of the photoresist 212 and 214 enables to selectively etch the underlying layers when using suitable process conditions. Therefore, a plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain electrodes 175 as well as a plurality of ohmic contact stripes 161 including a plurality of projections 163, a plurality of ohmic contact islands 165 and a plurality of semiconductor stripes 151 including a plurality of projections 154 are obtained by a series of etching steps.

[0099] For descriptive purpose, portions of the conductive layer 170, the extrinsic a-Si layer 160, and the intrinsic a-Si layer 150 on the wire areas A are called first portions, portions of the conductive layer 170, the extrinsic a-Si layer 160, and the intrinsic a-Si layer 150 on the channel areas C are called second portions, and portions of the conductive layer 170, the extrinsic a-Si layer 160, and the intrinsic a-Si layer 150 on the remaining areas B are called third portions.

[0100] An exemplary sequence of forming such a structure is as follows:

(1) Removal of third portions of the conductive layer 170, the extrinsic a-Si layer 160 and the intrinsic a-Si layer 150 on the wire areas A;

(2) Removal of the second portions 214 of the photoresist;

(3) Removal of the second portions of the conductive layer 170 and the extrinsic a-Si layer 160 on the channel areas C; and

(4) Removal of the first portions 212 of the photoresist.

[0101] Another exemplary sequence is as follows:

(1) Removal of the third portions of the conductive layer 170;

(2) Removal of the second portions 214 of the photoresist;

(3) Removal of the third portions of the extrinsic a-Si layer 160 and the intrinsic a-Si layer 150;

(4) Removal of the second portions of the conductive layer 170;

(5) Removal of the first portions 212 of the photoresist; and

(6) Removal of the second portions of the extrinsic a-Si layer 160.

[0102] The first example is described in detail.

[0103] As shown in Figs. 16A and 16B, the exposed third portions of the conductive layer 170 on the remaining areas B are removed by wet etching with the etchant used for the gate lines 121 and the storage electrode lines 131 to expose the underlying third portions of the extrinsic a-Si layer 160.

[0104] Reference numeral 174 indicates portions of the conductive layer 170 including the data lines 171 and the drain electrode 175 connected to each other. The dry etching may etch out the top portions of the photoresist 212 and 214.

[0105] Referring to Figs. 17A and 17B, the third portions of the extrinsic a-Si layer 160 on the areas B and of the intrinsic a-Si layer 150 are removed preferably by dry etching and the second portions 214 of the photoresist are removed to expose the second portions of the conductors 174. The removal of the second portions 214 of the photoresist are performed either simultaneously with or independent from the removal of the third portions of the extrinsic a-Si layer 160 and of the intrinsic a-Si layer 150. Residue of the second portions 214 of the photoresist remained on the channel areas C is removed by ashing.

[0106] The semiconductor stripes 151 are completed in this step, and reference numeral 164 indicates portions of the extrinsic a-Si layer 160 including the ohmic contact stripes and islands 161 and 165 connected to each other, which are called "extrinsic semiconductor stripes."

[0107] As shown in Figs. 18A and 18B, the second portions of the conductors 174 and the extrinsic a-Si stripes 164 on the channel areas C as well as the first portion 212 of the photoresist are removed.

[0108] As shown in Fig. 18B, top portions of the projections 154 of the intrinsic semiconductor stripes 151 on the channel areas C may be removed to cause thickness reduction, and the first portions 212 of the photoresist are etched to a predetermined thickness.

[0109] In this way, each conductor 174 is divided into a data line 171 and a plurality of drain electrodes 175 to be completed, and each extrinsic semiconductor stripe 164 is divided into an ohmic contact stripe 161 and a plurality of ohmic contact islands 165 to be completed.

[0110] As shown in Figs. 19A-19C, a passivation layer 180 is deposited and patterned to form a plurality of contact holes 182, 185 and 189 exposing expansions 125 of the gate lines 121, the drain electrodes 175, and expansions of the data lines 171.

[0111] Finally, as shown in Figs. 10-12, an IZO layer with a thickness in a range between about 500Å and about 1,000Å is sputtered and photo-etched using the etchant used for the gate lines 121 and the data lines 171 to form a plurality of pixel electrodes 190 and a plurality of contact assistants 92 and 97.

[0112] This embodiment simplifies the manufacturing process by forming the data lines 171 and the drain electrodes 175 as well as the ohmic contacts 161 and 165 and the semiconductor stripes 151 and using a single photolithography step.

[0113] A TFT array panel for an LCD according to another embodiment of the present invention will be described in detail with reference to Figs. 20 and 21.

[0114] Fig. 20 is a layout view of an exemplary TFT array panel for an LCD according to another embodiment of the present invention, and Fig. 21 is a sectional view of the TFT array panel shown in Fig. 20 taken along the line XXVII-XXVII'.

[0115] As shown in Figs. 20 and 21, a layered structure of a TFT array panel of an LCD according to this embodiment is almost the same as that shown in Figs. 4 and 5. That is, a

plurality of gate lines 121 including a plurality of gate electrodes 123 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of contact holes 182 and 189 exposing expansions 125 and 179 of the gate lines 121 and the data lines 171 are provided at the passivation layer 180 and/or the gate insulating layer 140, and a plurality of pixel electrodes 190 and a plurality of contact assistants 92 and 97 are formed thereon.

[0116] Different from the TFT array panel shown in Figs. 4 and 5, the data lines 171 and the drain electrodes 175 includes a bottom layer 171p preferably made of Mo or Mo alloy, an intermediate layer 171q preferably made of Al or Al alloy, and a top layer 171r preferably made of Mo or Mo alloy.

[0117] Now, a method of manufacturing the TFT array panel shown in Figs. 20 and 21 according to an embodiment of the present invention will be described in detail with reference to Figs. 22A-32 as well as Figs. 20 and 21.

[0118] Figs. 22A, 23A, 24A and 25A are layout views of the TFT array panel shown in Figs. 20 and 21 in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention, and Figs. 22B, 23B, 24B and 25B are sectional views of the TFT array panel shown in Figs. 22A, 23A, 24A and 25A taken along the lines VIB-VIB', VIIB-VIIB', VIIIB-VIIIB', and IXB-IXB', respectively.

[0119] Two conductive films, a lower conductive film and an upper conductive film are

sputtered in sequence on an insulating substrate 110 such as transparent glass. The lower conductive film has a thickness of about 1,500-3,000 Å, preferably 2,500 Å and is made of Al-Nd alloy, while the upper conductive film has a thickness of about 300-600 Å, preferably 500 Å and is made of Mo.

[0120] Referring to Figs. 22A and 22B, the upper conductive film and the lower conductive film are simultaneously patterned by photolithography and wet etch with an etchant to form a plurality of gate lines 121 including a plurality of gate electrodes 123, a plurality of projections 127, and a plurality of expansions 125. The etchant contains about 65-75% H_3PO_4, about 0.5-4% HNO_3, about 9-13% CH_3COOH, about 2-5% stabilizer, and deionized water. The stabilizer includes oxy-hydride inorganic acid represented by $M(OH)_XL_Y$, where M is Zn, Sn, Cr, Al, Ba, Fe, Ti, Si or B, L is H_2O, NH_3, CN or NH_2R (where R is alkyl group), X is 2 or 3, and Y is 0, 1, 2 or 3. Although the elements contained in the etchant are the same as those described with reference to Figs. 6A and 6B, the percentages thereof are different since the materials forming the gate lines 121 are different.

[0121] Referring to Figs. 23A and 23B, after sequential deposition of a gate insulating layer 140, an intrinsic a-Si layer, and an extrinsic a-Si layer, the extrinsic a-Si layer and the intrinsic a-Si layer are photo-etched to form a plurality of extrinsic semiconductor stripes 164 and a plurality of intrinsic semiconductor stripes 151 including a plurality of projections 154 on the gate insulating layer 140.

[0122] Referring to Figs. 24A and 24B, a bottom film made of Mo, an intermediate film made of Al-Nd alloy, and a top film made of Mo are sequentially deposited and wet-etched with the etchant used for patterning the gate lines 121 to form a plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of expansions 179, a plurality of drain

electrodes 175, and a plurality of storage capacitor conductors 177.

[0123] Thereafter, portions of the extrinsic semiconductor stripes 164, which are not covered with the data lines 171, the drain electrodes 175, and the storage capacitor conductors 177, are removed to complete a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 and to expose portions of the intrinsic semiconductor stripes 151. Oxygen plasma treatment preferably follows thereafter in order to stabilize the exposed surfaces of the semiconductor stripes 151.

[0124] Referring to Figs. 25A and 25B, a passivation layer 180 is deposited and the passivation layer 180 and the gate insulating layer 140 are photo-etched to form a plurality of contact holes 182, 185, 187 and 189 exposing the expansions 125 of the gate lines 121, the drain electrodes 175, the storage capacitor conductors 177, and the expansions 179 of the data lines 171.

[0125] Finally, as shown in Figs. 20 and 21, a plurality of pixel electrodes 190 and a plurality of contact assistants 92 and 97 are formed on the passivation layer 180 by sputtering and photo-etching an IZO layer having a thickness of about 800-1,000 Å, preferably 900 Å with the etchant used for etching the gate lines 121 and the data lines 175.

[0126] According to another embodiment of the present invention, a plurality of color filters (not shown) are provided under the pixel electrodes.

[0127] As described above, the gate lines 121, the data lines 171, and the pixel electrodes 190 are etched by using a single etchant with elements having percentages depending on materials to be etched. Accordingly, the manufacturing method and apparatus are simplified, thereby reducing the manufacturing cost.

[0128] While the present invention has been described in detail with reference to the

preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.